The project implemented Internal Logic Analyzer, a checking device which assist debugging the FPGA card. The device is independent in the manufacturer of the card. The project was written in VHDL code. Both entering data into the system and extracting it are according to UART protocol.

In the system there is a possibility for the user to define the depth and the width of the recorded data as he wishes, also he can define trigger type(out of four defined options) and determine the trigger positin.